5. Description of Function

5.1 General

Refer to block diagram 564.4018FS in the appendix to this manual.

Reception Signal Path

The Rx section is based on a modern concept with a high 1st IF and with fixed tuned filters exclusively. All auxiliary carriers are derived from a precision oscillator that is thermostat controlled.

The antenna signal is fed to the preselection filters which are automatically switched depending on the frequency tuning. Depending on the model, the preselection consists either of a low-pass filter (10 kHz to 1.5 MHz), or of a band-pass filter (0.5 to 1.5 MHz), and between 1.5 and 30 MHz out of a high-pass filter (basic model) or of eight staggered sub-octave filters. These sub-octave filters reduce effectively 2nd order intermodulation products and suppress distant noise sources.

Conversion/Selection

The conversion to the 1st IF frequency of 81.4 MHz is accomplished with the synthesizer output frequency that is variable in 10-Hz steps.

The selection in the 1st IF is performed by a crystal filter, 12 kHz broad that determines the maximum input bandwidth. Three (basic model) or eight further crystal filters are available in the 2nd IF (1.4 MHz) that can be switched into circuit as required.

Optimum adaptation to reception conditions and type of emission is allowed for by the logarithmic bandwidth staggering.

Amplification/Control

Since the control voltage is strictly proportional to the amplification factor of the multi-stage IF amplifier it is also used as a direct indication for the signal voltage at the antenna. The voltage is indicated on the control panel following digitising. The amplification control of the receiver may be executed either by hand, automatically or by remote control.

Demodulation/Connections

The IF signal is converted into the AF state with AM transmissions by an envelope curve rectifier and with CW, SSB (A1A, A1B, J3E) and AFSK signals by the BFO switchable in 100-Hz steps. For FSK demodulation the IF signal is further amplified, limited and phase demodulated. After differenciation a keying stage generates single-current signals for direct connection to a teletype and double-current signals acc. to CCITT V.28. Further the FSK demodulator controls the tuning indicator.

Control by Microprocessor

Depending upon the settings on the control panel the processor provides and processes the data for all modules of the receiver.

Data Interface Function

With remotely controlled models the external data bus transfer is performed either via the IEC bus connection or via an interface acc. to CCITT (V.24, switchable to V.10 for remote control over average distances without modem) depending on model.

5.2 Control Panel

5.2.1 Control Panel with LED Display (B3)

Refer to Fig. 5.1 and circuit diagram 566.0810S

All displays are driven by data (2 x 4 bits) and an address (4 bits). The addresses are decoded into 1-out-of-16 code. The data are stored in the appropriate latch (memory flip-flop) by the individual strobe signals. A built-in decoder drives the LED displays.

The code for the LEDs in the keys is also stored in latches. The LEDs are driven by driver stages.

The key matrix is driven in the X direction by eight strobe lines with coding derived from the address. The eight lines in the Y-direction are the return lines and signal which key is pressed.

The level is indicated by a meter preceded by an impedance transformer.

The analog voltage for indicating frequency shift is converted into 1-out-of-21 code by an A/D converter. This drives the LED spot display directly.

The quasi-continuous frequency tuning works with a pulse train. This is produced by optical scanning of a rotatable grid aperture disk by two light barriers. There are two pulse trains offset in phase by 90° to enable recognition of the direction of rotation.

The AF signal goes by way of a switch directly to the loudspeaker and across an attenuator to the headphones jack.

The brightness of the displays is regulated with a control circuit and can be adjusted with the knob 17.

The RF control 28, AF control 20, LOCal/REMote switch 30, LOCK button 18 and POWER lamp 14 are connected directly to the associated modules.

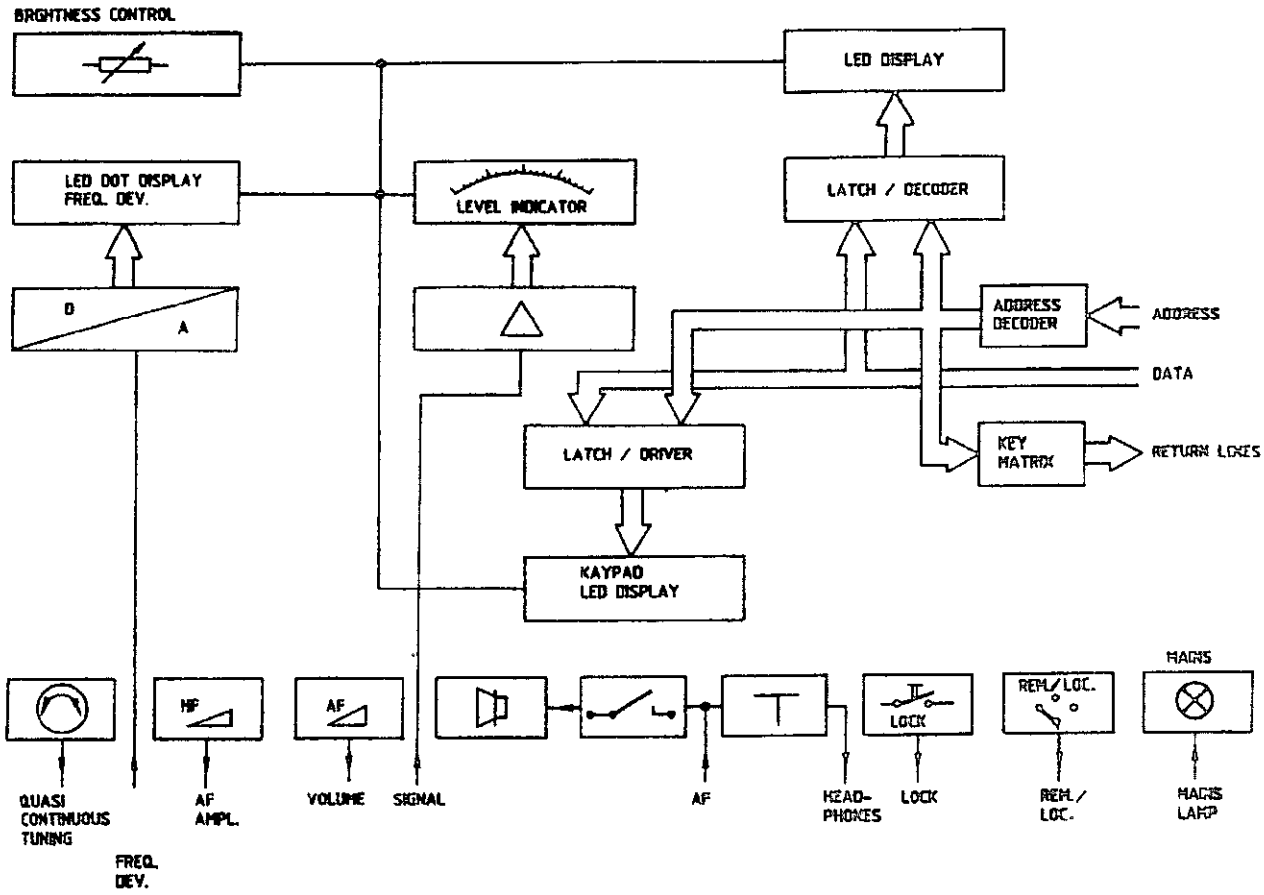

Fig. 5.1 Control Panel with LED Display (B3), Block Diagram

5.2.2 Control Panel with LCD Display (B2)

Refer to Fig. 5.2 and circuit diagram 565.9613S

All displays are driven by data (2 x 4 bits) and an address (4 bits). The addresses are decoded into 1-out-of-16 code. The data are stored in the appropriate latch by the individual strobe signals. A built-in LCD decoder drives the LCD displays, which have conductive rubber contacts.

The code for the LEDs in the keys is also stored in latches. The LEDs are driven by driver stages.

The key matrix is driven in the X direction by eight strobe lines with coding derived from the address. The eight lines in the Y direction are the return lines and signal which key is pressed.

The LEVEL bargraph display is produced by code conversion from the digital LEVEL display.

The analog voltage for indicating frequency shift is converted into an 8-bit code by a CMOS A/D converter. The 8-bit code is then recoded for driving an LCD spot display.

The heating for all the LCD displays comes from a very thin metal plate, vapour-deposited onto the rear of the glass plates. The switching on and off of this heating is controlled by a temperature sensor (NTC resistor). The heating only cuts in at temperatures of less than +10° C.

The quasi-continuous frequency tuning works with a pulse train. This is produced by optical scanning of a rotatable grid aperture disk by two light barriers. There are two pulse trains offset in phase by 90° in order to determine the rotation direction.

The AF signal goes by way of a switch directly to the loudspeaker and across an attenuator to the headphones jack.

The illumination is switched on and off with a slide switch. The switch is bypassed with a resistor for preheating the lamps and thus avoiding a current inrush.

The RF control, AF control 20, LOCal/REMote switch 30, LOCK button 18 and POWER lamp 14 are connected directly to the associated modules.

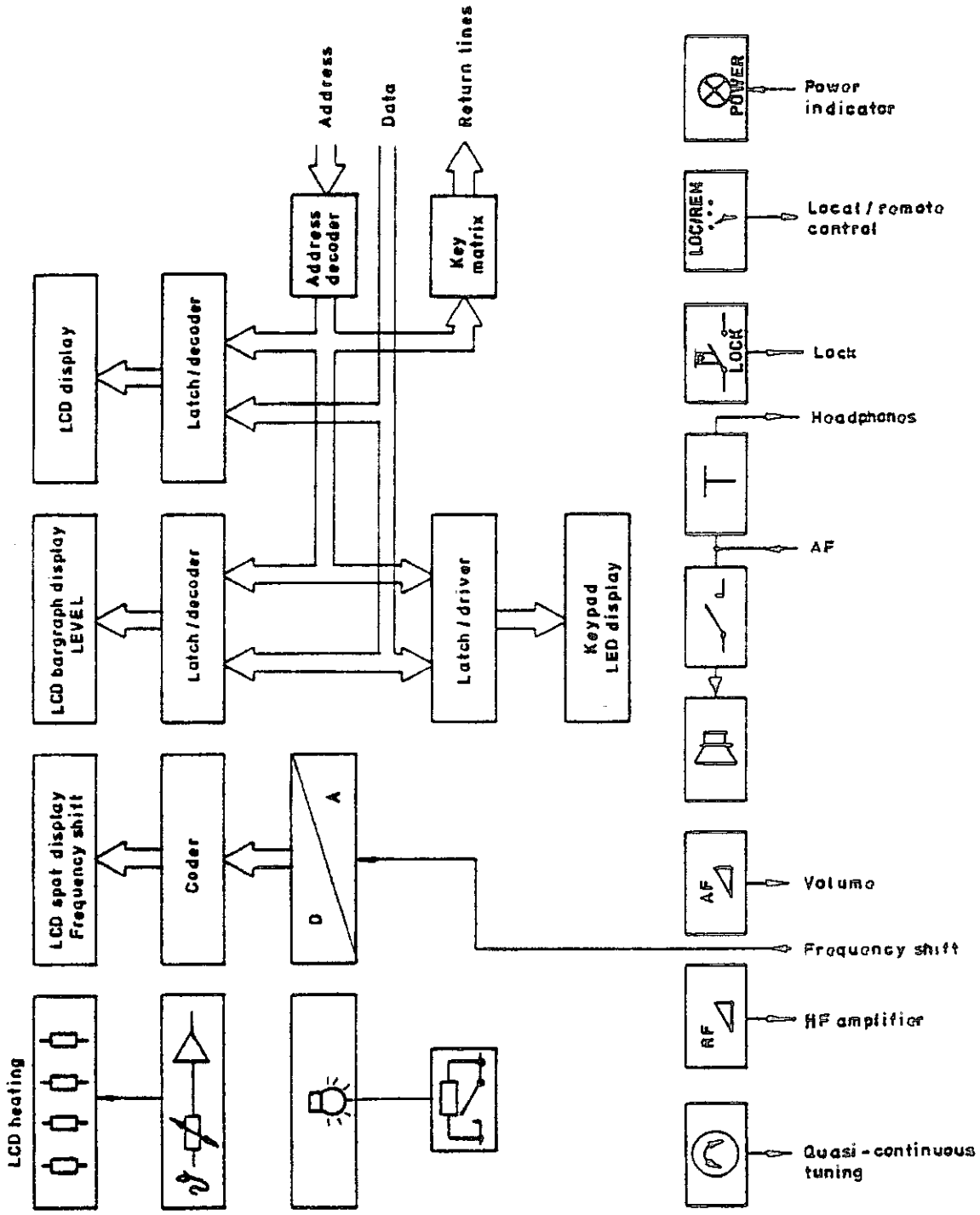

Fig. 5.2 Control Panel with LCD Display (B2), Block Diagram